



MyVHDL Station V4.0x Tutorial

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Preface

1. What is MyCAD ?

MyCAD is set of Electronic Design Automation (EDA) tools developed by Seodu Logic, Inc. Along the world-wide trend of EDA tools downsizing in 1990s, **MyCAD** tool set targets the best EDA tools on PC platforms. **MyCAD** tools are being used for VHDL modeling logic synthesis, digital logic design, FPGA design, PLD design, analog circuit design, IC layout design and verification, and PCB (Printed Circuit Board) layout design.

2. MyCAD Tools Environment

The design of a circuit is initiated from an idea concept of the circuit. One of the **MyCAD** tools, **MyVHDL**, is used to implement the circuit by high level language for modeling and simulation of the circuit.

After simulation is completed, the design represented by high level language is converted to logic gates in terms of **MyCAD**'s MySynthesis Station. **MySynthesis** is a logic optimization tool, and synthesizes logic gates from the circuitry designed by **MyVHDL**.

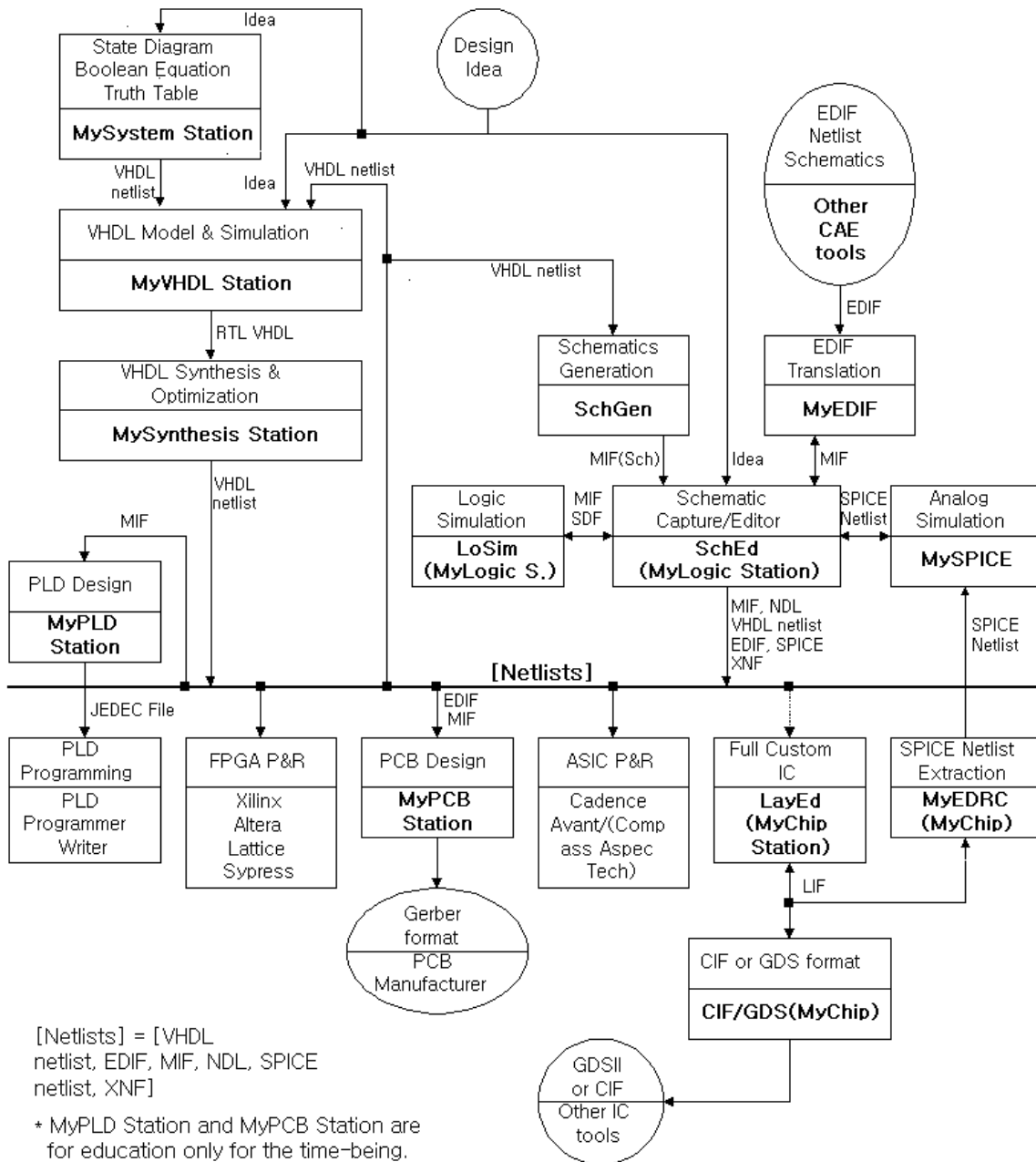
Currently **MyVHDL** and **MySynthesis** can be applied again to the input of **MyVHDL**, or to SchEd (schematic Editor) via SchGen (schematic generator).

Furthermore, the data can be shared by Logic Station, which is a design tool for FPGA (Field Programmable Gate Array), ASIC (Application Specific Integrated Circuit) or FCIC (Full Custom IC) designs. The flow between each tool is simple and closely coupled, and sometimes requires a few more steps. Direct drawing of schematics is also one method of designing circuitry without using high level design language.

MyLogic Station which includes schematic editor can be used for the purpose. The schematic design is verified by the logic simulator, MySim. The design after simulation can be transported to FPGA, ASIC or FCIC.

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The diagram of MyCAD Tools Environment



Chap. 1 The installation of MyVHDL Station

1.1 System Requirement

- . System : IBM PC compatible Pentium 90 or faster
- . HDD free space : at least 50MB
- . Memory : at least 16MB, 32MB of more recommended
- . Operating System : Windows 95/98, Windows NT
- . External C-Compiler : MS Visual C++ V5.0

1.2 How to Install

1.2.1 Run setup program

Put CD-ROM in your CD-ROM drive. The auto-run feature will automatically run install program. Then, click with the left mouse button. If the auto-run dose not work, run the installation program named *setup.exe* on the root directory of the CD-ROM. Then, proceed the installation.



If you download MyVHDL education version which is provided from our web site, you have to run the installation

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program of MyVHDL Station named `setup_vhdl.exe`. Then, the following dialog box will be shown.



To proceed, click `Next` with the left mouse button.

Note: If you run the installation program of MyVHDL, `setup_vhdl.exe` the process of installation will move to 1.2.4.

1.2.2 Select MyVHDL Station at 'Select Component' List Box

Select MyVHDL Station at *Program* list box by clicking with the left mouse button.

Then, click `Next` with left mouse button to proceed.



1.2.3 Select License Scheme at *Select License Scheme* dialog box

Select License Scheme at *license scheme* list box.

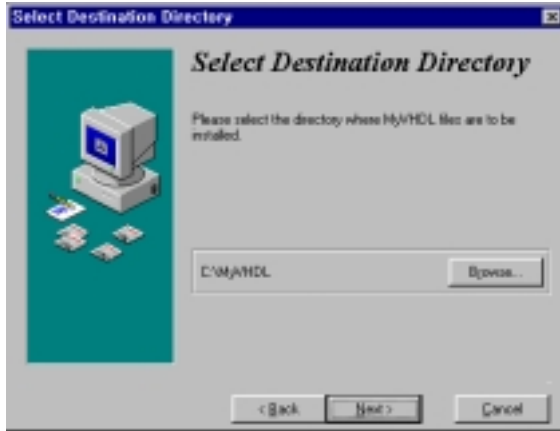
Note: Please confirm your license scheme before select it at *license scheme* list box.

Then, click `Next` with left mouse button to proceed.



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1.2.4 Specify the installation directory



If you want to change directory, click **Browse**. Then, following dialog box will be shown.

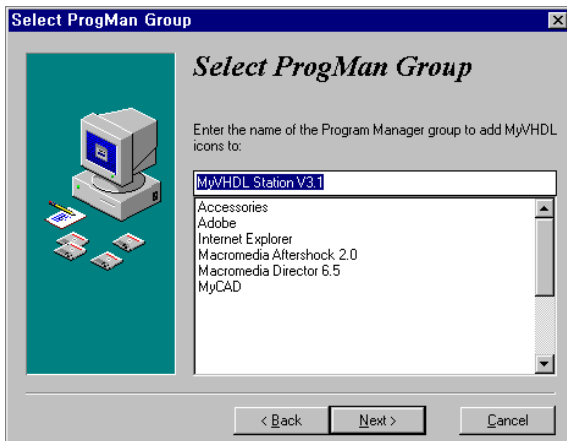


Specify the

installation directory at above directory dialog box.

Note: If you do not specify the installation directory, the default installation directory will be set to C:\MyCAD

1.2.5 Specify Program Group

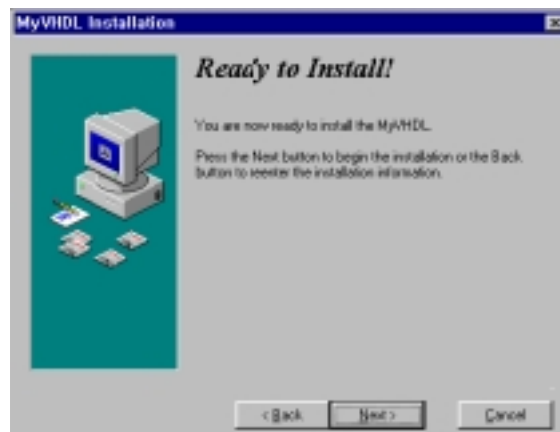


Specify program group name at *Select ProgMan group* dialog box.

Note: If you do not specify the group name, the default program group will be named to **MyCAD 1999**

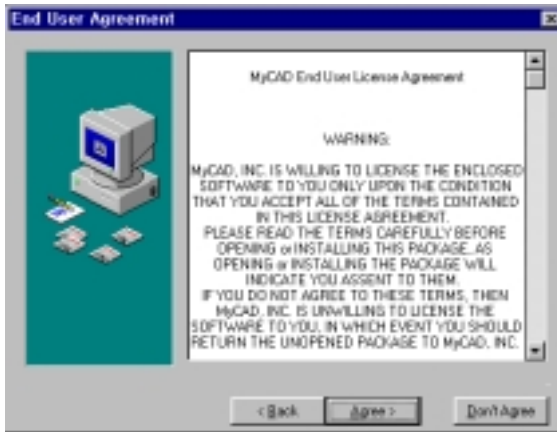
Then, click **Next** with left mouse button to proceed.

To proceed, click **Next** with left mouse button at *Ready to Install* dialog box.



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1.2.6 Review the agreement

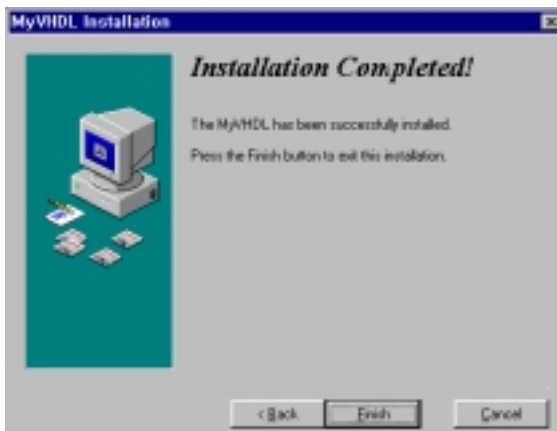


After finishing the installation, MyCAD End User License Agreement will be shown.

Click *Agree*, then you will see the process of installation.



1.2.7 Complete installation



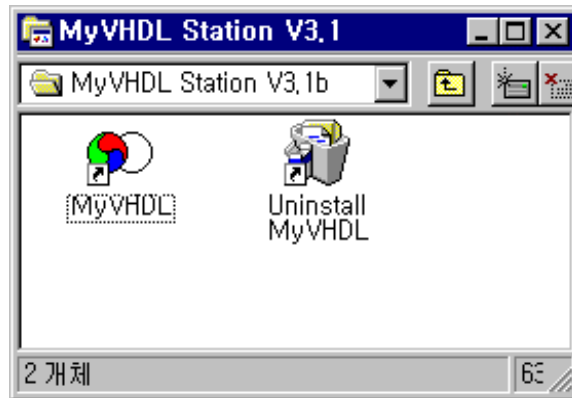
To complete installation, click Finish

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1.3 The constructs of MyVHDL Station

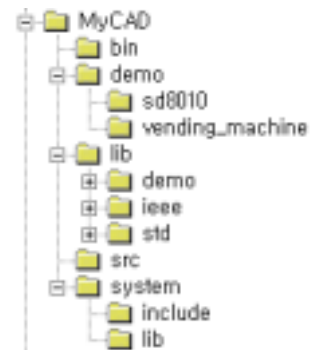
1.3.1 MyVHDL Program ICON

Add two program icons to **MyCAD 1999** program icon group. One, **MyVHDL**, is to run **MyVHDL**. The other is to run uninstall process. If you install the education program, **MyVHDL Station V3.1b** program icon group will make as following diagram.



1.3.2 The Directory Structure of MyVHDL

- Bin : Executable files and dll files to run **MyVHDL**
- Demo : Demo designs for **MyVHDL**
- Lib : IEEE Standard Libraries & User Defined Libraries
- Src : VHDL Source Files of IEEE Standard Libraries
- System : files used to compile VHDL files.



Chap. 2 Starting Up MyVHDL Station

2.1 Overview

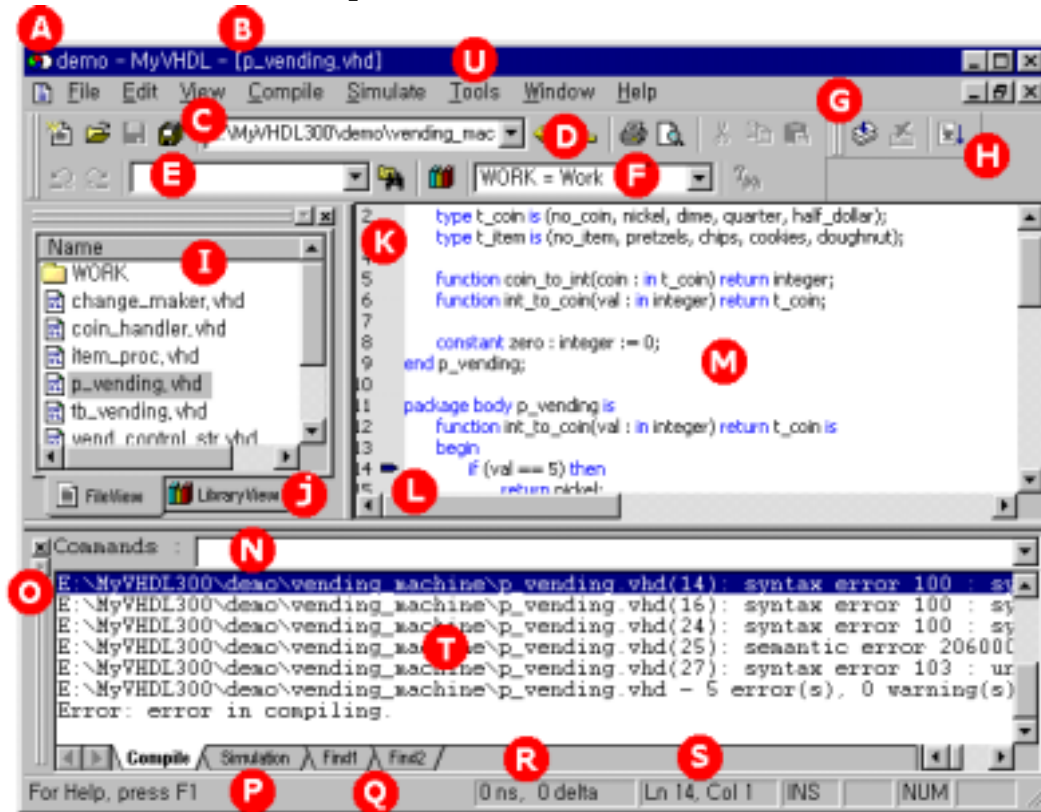
To compile VHDL source code with MyVHDL Station, you have to install MS Visual C++ V5.0. MyVHDL generate c-code files during compile VHDL source code. To proceed, need c-compiler. MS Visual C++ V5.0 is only available to compile c-code files that are generated during compile VHDL source code at MyVHDL Station.

Note: If you use the evaluation version of MyVHDL Station, it is available only a month to use and until 100ns to simulate.



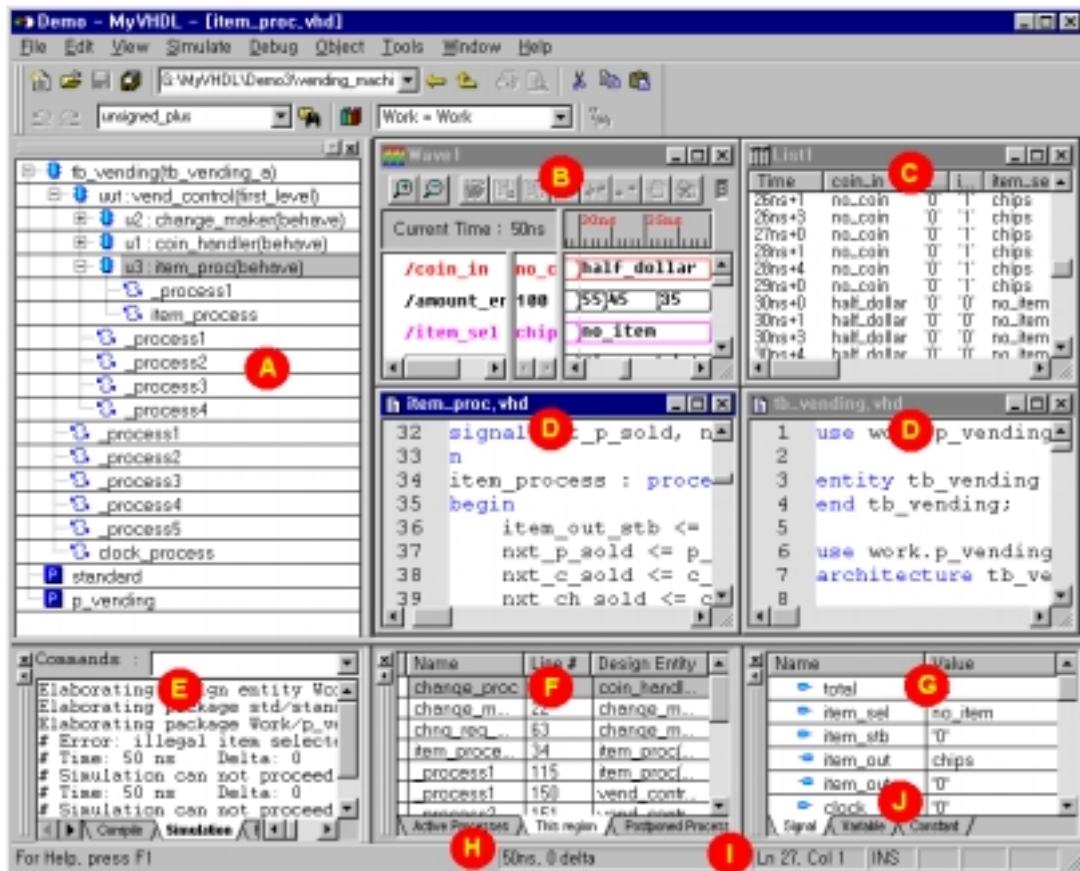
2.2 GUI (Graphic User Interface)

2.2.1 Compile Mode Windows



- | | |
|-------------------------------------|----------------------------|
| A - Project name | K - Source Line number |
| B - VHDL Source file name | L - Source indicator |
| C - Current directory path | M - Source Window |
| D - Change directory button | N - Command View |
| E - Find view | O - VHDL Analysis Message |
| F - Selected Library | P - Simulation message tag |
| G - Compile button | Q - Find message tag |
| H - Simulation button | R - Simulation time |
| I - Project window (directory tree) | S - Source Editor point |
| J - Library window tag | T - Message window |

2.2.2 Simulation/Debug Mode Windows



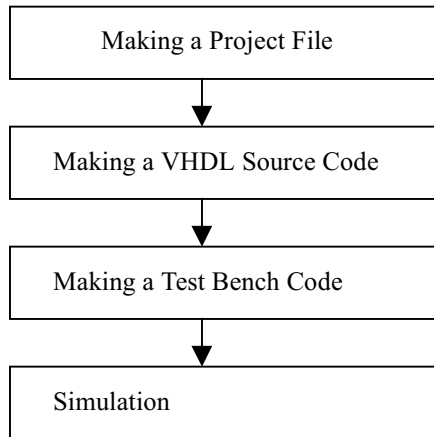
A-

- Design Manager
- B – Wave Window
- C – List Window
- D – Source Window
- E – Simulation Output Window
- F – Process View Window
- G – Object View Window
- H – Simulation Time
- I – Current Position
- J – Object Select Tag

2.3 MyVHDL Station Job Flow

The following diagram shows a job flow using MyVHDL Station.

The box denotes the procedure that is performed by user.



2.3.1 Making a Project

Project file contains the information about the environment of MyVHDL Station and associated VHDL file name.

To make a project file, just following next sequences

1. Choose **File** → **New** at pop-up menu of MyVHDL.
2. Select Project at New dialog box.
3. For more, refer to 3.3.

An example of project file is shown below.

```
[MyVHDL300_PROJECT_FILE]
(object
  (objectName (STRING "project"))
  (objectType (STRING "PROJECT"))
  (objectXID (XID 1))
  (library
    (libraryName (STRING "std"))
    (libraryPath (STRING "%STD%\std.mv1"))
```

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```
(setWork (BOOLEAN FALSE))
)
(library
  (libraryName (STRING "ieee"))
  (libraryPath (STRING "%IEEE%\ieee.mv1"))
  (setWork (BOOLEAN FALSE))
)
(library
  (libraryName (STRING "Work"))
  (libraryPath (STRING "%MyVHDL%\Demo\Work\Work.mv1"))
  (setWork (BOOLEAN TRUE))
)
)
```

2.3.2 Making a VHDL Source Code

To make a VHDL source code, just follow next sequences.

1. Choose *File* → *New* at pop-up menu of MyVHDL.
2. Select VHDL at New dialog box.
3. For more, refer to 3.3.

2.3.3 Making a Test Bench Code

To make a Test Bench code, just follow next sequences.

1. Choose *File* → *New* at pop-up menu of MyVHDL.
2. Select VHDL at New dialog box.
3. For more, refer to MyVHDL User's Guide.

2.3.3 Simulation

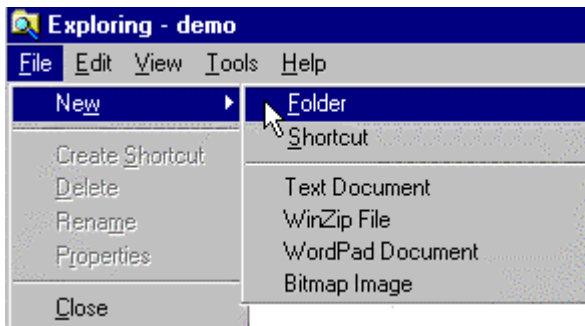
To simulate VHDL source code, refer to 3.4 and 3.5 or MyVHDL User's Guide.

3. LAB: Full Adder Design

In this lab, we will explain how to use MyVHDL through full adder design. Full adder is composed of two half adders and a OR gate. And half adder is composed of an AND gate and an XOR gate.

The first step of using MyVHDL is to make a directory at Windows Explorer to maintain the example data.

At *C:\mycad\demo\myvhdl directory*, click *OK* the right button to bring up the pop-up menu and then select *New → Folder*.



Then type the name of directory as FA.



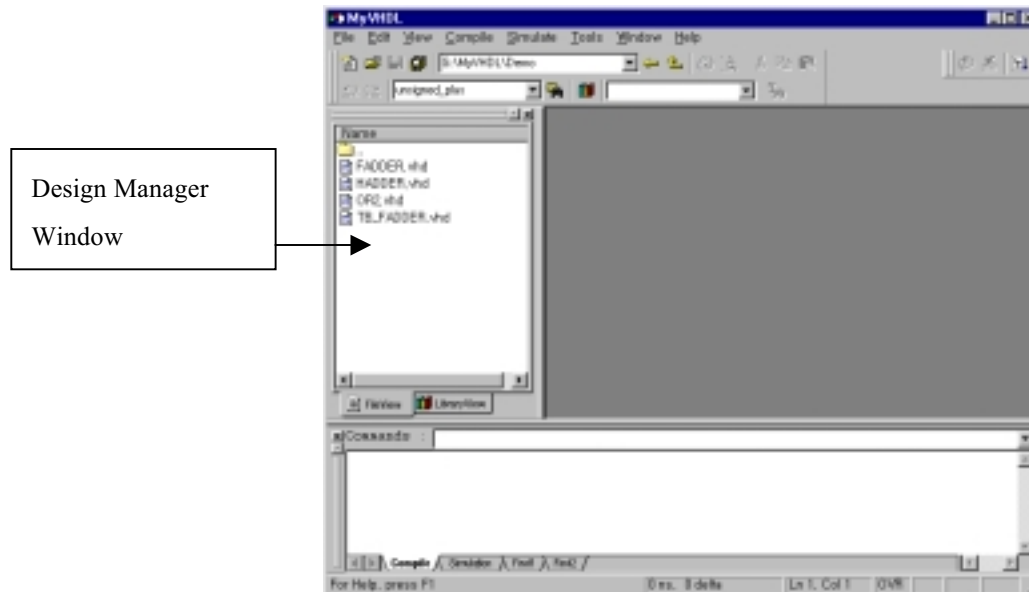
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3.1 Run MyVHDL

To run MyVHDL, click MyVHDL icon with the left mouse button at MyVHDL program icon group. Then, the log window above will be shown.

3.2 Move to your job directory

To move to your job directory, choose the directory at *Design Manager window* of MyVHDL.

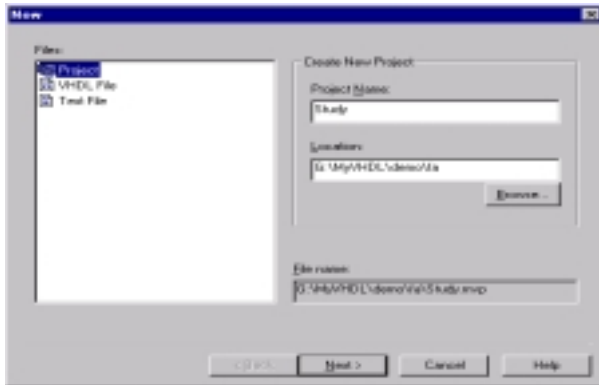


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3.3 Make a Project File

To make a project file, just follow from step 1 to step 7.

Step 1. Choose *File* → *New* at pop-up menu of MyVHDL. Then following dialog box will be shown.



Step 2. Select *Project* from *Files* selection box. Then, type 'Study' at *Project Name* text box.

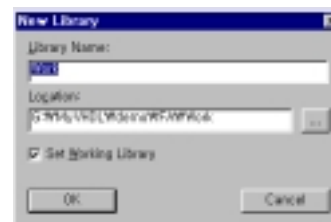
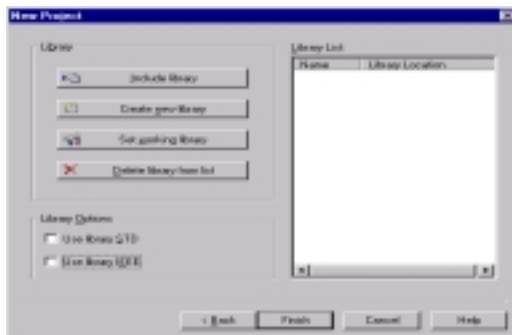
You will see the project file name and location at '*File name*' text box after finishing step 1 and step 2.

Note: If you want to specify the location of project file, specify the location by typing absolute path at *Location* text box or by clicking *Browse* button and locating.

Step 3. Choose *Next* button with the left mouse button. *New Project* dialog box will be shown.

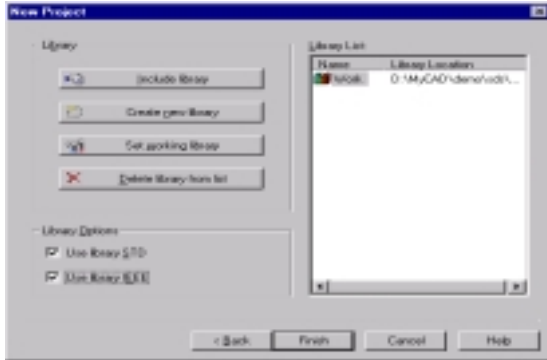
Step 4. Choose *Create new Library* with the left mouse button, Then *New Library* dialog box will be shown. Type Library name '*Work*' at *Library Name* text box.

Check in *Set Working Library*.



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Step 5. Choose 'OK' at New Library dialog box. Then, add your Work Library to Library List Box.



Step 6. Check in both *Use library STD* and *Use library IEEE* at Library Options list box.

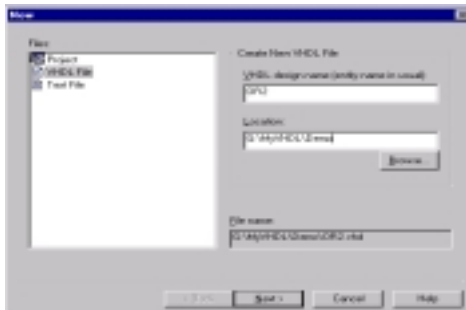
Step 7. Click *Finish* button.

3.3 Making a VHDL Source File

MyVHDL provide VHDL Source Code Wizard. To make a VHDL source file, just follow from step 1 to step 11. To make OR gate VHDL Source Code, use VHDL Source Code Wizard.

3.3.1 OR gate design

Step 1. Choose *File*→*New* at pop-up menu of MyVHDL. Then, New dialog box will be shown. Select *VHDL File* from Files list box.



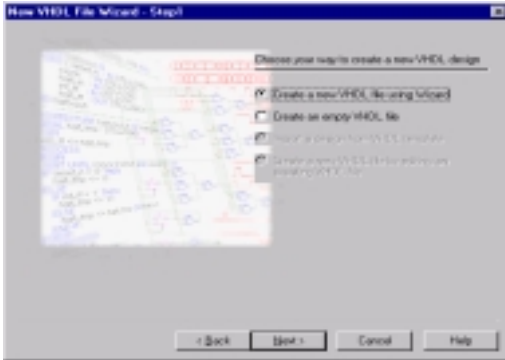
Step 2. Type OR2 at VHDL design name (entity name in usual) text input box.

Specify the location of VHDL source code by typing absolute path or by clicking Browse button and location at Location text input box. And click *Next*.

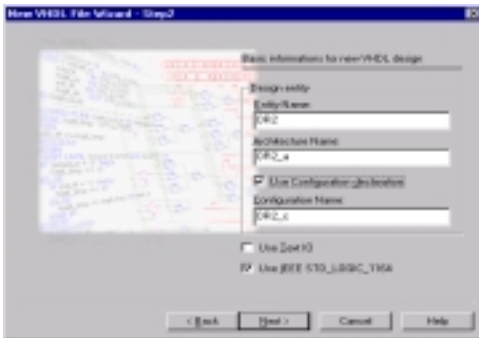
Step 3. New VHDL File Wizard – Step 1 dialog box will be shown. Choose *Create a new VHDL file using Wizard* from List box
Choose your way to create a new VHDL design. List box

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Click *Next*, then VHDL File Wizard – Step 2 dialog box will be shown.



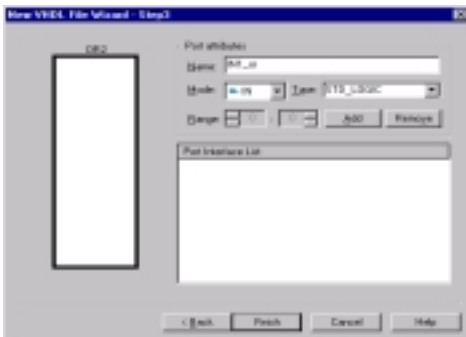
Step 4. You can use special names to specify entity name at Entity Name text input box, architecture name at Architecture Name text input box, and configuration name at Configuration Name text input box.



Note: In general, MyVHDL wizard provides the default values.

Step 5. To use **IEEE.STD_LOGIC_1164** libraries at your VHDL source code. You have to check in 'Use IEEE STD_LOGIC_1164'.

Step 6. Click *Next* with left mouse button, then VHDL File Wizard – Step 3 dialog box will be shown. Specify port attribute name 'IN_or' at Port attributes input box.

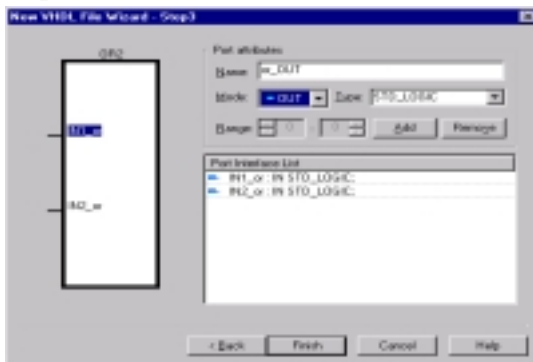


Step 7. Specify port's mode 'IN' at Mode box and port's type 'STD_LOGIC' at Type box..

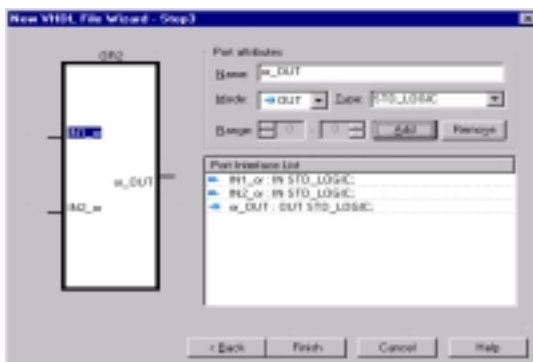
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Step 8. Click *Add* with the left mouse button to proceed. Then you can add a new port to VHDL Source Code.



Step 9. After adding ports to VHDL Source Code, you will see the result as following diagram.



Step 10. If you want to finish adding all ports, click *Finish* with the left mouse button.

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Step 11. Then, you will get a VHDL Source Code as shown below.

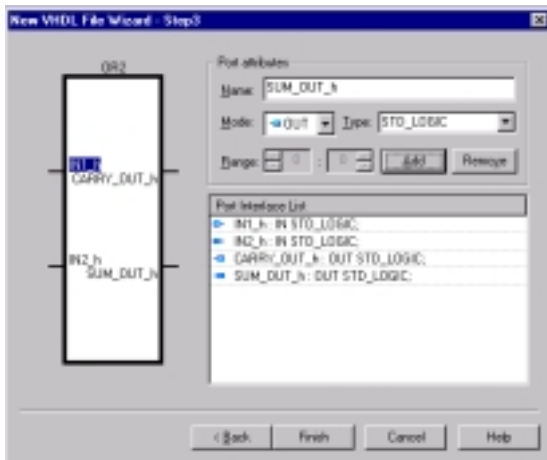
In this VHDL Source Code which is driven by VHDL Source Code Wizard, you have to add your specialized code to blank field like as following.

Note: Refer to bold characters at VHDL Source Code.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY OR2 IS
    PORT(
        IN1_or : IN STD_LOGIC;
        IN2_or : IN STD_LOGIC;
        or_OUT : OUT STD_LOGIC
    );
END OR2
--BEGIN
    --TODO: Add your specialized code here.
ARCHITECTURE OR2_a OF OR2 IS
BEGIN
    -- TODO: Add your specialized code here.
    PROCESS(IN1_or, IN2_or)
    BEGIN
        IF IN1_or = '1' or IN2_or = '1' then
            or_OUT <= '1';
        ELSE
            or_OUT <= '0';
        END IF;
    END PROCESS;
END OR2_a;
CONFIGURATION OR2_c OF OR2 IS
    --TODO: Add your specialized code here.
    FOR OR2_A
    END FOR;
END OR2_c;
```

3.3.2 Half Adder Design

To make a half adder VHDL Source Code, refer to section 3.3.1. Then add your specialized code to blank field like as following.



Note: Refer to bold characters at VHDL Source Code.

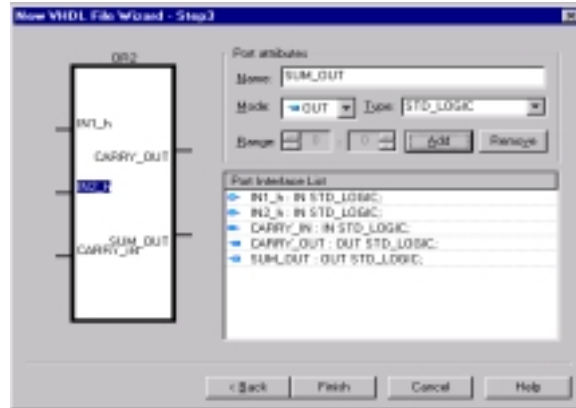
```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY HADDER IS
    PORT(
        IN1_h : IN STD_LOGIC;
        IN2_h : IN STD_LOGIC;
        CARRY_OUT_h : OUT STD_LOGIC;
        SUM_OUT_h : OUT STD_LOGIC
    );
END HADDER;
ARCHITECTURE HADDER_a OF HADDER IS
BEGIN
    -- TODO: Add your specialized code here.
    PROCESS(IN1_h, IN2_h)
    BEGIN
        CARRY_OUT_h <= IN1_h AND IN2_h;
        SUM_OUT_h <= IN1_h XOR IN2_h;
    END PROCESS;
END HADDER_a;
```

```
END PROCESS;  
END HADDER_a;  
CONFIGURATION HADDER_c OF HADDER IS  
    -- TODO: Add your specialized code here.  
    FOR HADDER_a  
    END FOR;  
END HADDER_c;
```

3.3.3 Full Adder Design

Finally, lets make full adder VHDL source Code.
To make a half adder VHDL Source Code, refer to section 3.3.1. Then add your specialized code to blank field like as following.

Note: Refer to bold characters at following VHDL source Code.



```
ARCHITECTURE FADDER_a OF FADDER IS  
    COMPONENT HADDER  
        PORT ( IN1_h, IN2_h : IN STD_LOGIC;  
              CARRY_OUT_h, SUM_OUT_h : OUT STD_LOGIC);  
    END COMPONENT;  
    COMPONENT OR2  
        PORT ( IN1_or, IN2_or : IN STD_LOGIC;  
              or_OUT : OUT STD_LOGIC);  
    END COMPONENT;  
    SIGNAL tmp_carry1, tmp_carry2, tmp_sum : STD_LOGIC;  
BEGIN  
    U1 : hadder PORT MAP (IN1, IN2, tmp_carry1, tmp_sum);  
    U2 : hadder PORT MAP (tmp_sum, CARRY_IN, tmp_carry2, SUM_OUT);  
    U3 : or2 PORT MAP (tmp_carry1, tmp_carry2, CARRY_OUT);  
END FADDER_a;
```

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CONFIGURATION FADDER_c OF FADDER IS

FOR FADDER_a

FOR U1 : hadder USE ENTITY work.HADDER(HADDER_A);

END FOR;

FOR U2 : hadder USE ENTITY work.HADDER(HADDER_A);

END FOR;

FOR U3 : or2 USE ENTITY work.OR2 (OR2_A);

END FOR;

END FOR;

END FADDER_c;

3.3.4 Making a Test Bench

Before simulating VHDL Source Codes, you have to make bench file. Test bench Code is contained the information which need to simulate VHDL Source Code. To make test bench code, use text editor at 'Start → Run → Notepad'. and then, type as follow and save it named 'TB_Adder.vhd'.

LIBRARY IEEE;

USE IEEE.std_logic_1164.all;

ENTITY TB_FADDER is

END TB_FADDER;

ARCHITECTURE TB_FADDER_A of TB_FADDER is

SIGNAL IN1, IN2 : STD_LOGIC;

SIGNAL CARRY_IN : STD_LOGIC := '1';

SIGNAL CARRY_OUT, SUM_OUT : STD_LOGIC;

COMPONENT FADDER

PORT (IN1, IN2, CARRY_IN : IN STD_LOGIC;

CARRY_OUT, SUM_OUT : OUT STD_LOGIC);

END COMPONENT;

BEGIN

L1: FADDER

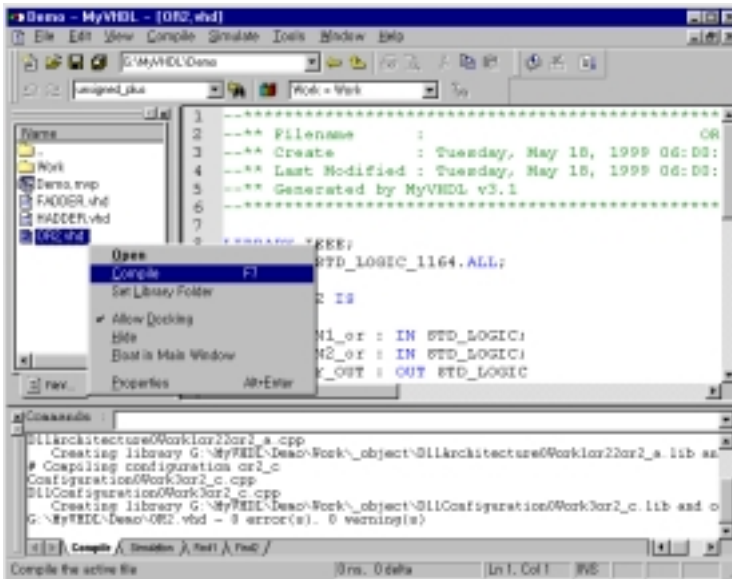
PORT MAP (IN1, IN2, CARRY_IN, CARRY_OUT, SUM_OUT);

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```
PROCESS
BEGIN
    WAIT FOR 40 ns; CARRY_IN <= NOT CARRY_IN;
END PROCESS;
PROCESS
BEGIN
    IN1 <= '1','0' after 10 ns,'1' after 20 ns, '0' after 30 ns,'1' after 40 ns, '0' after 50 ns,
           '1' after 60 ns, '0' after 70 ns,'1' after 80 ns, '0' after 90 ns;
    IN2 <= '1','0' after 15 ns,'1' after 30 ns, '0' after 45 ns,'1' after 60 ns,
           '0' after 75 ns, '1' after 90 ns, '0' after 105 ns;

    WAIT;
END PROCESS;
END FADDER_c;
```

3.5. VHDL Source Code Compile



To compile VHDL Source Code, choose *Compile* → *Compile* at pop-up menu of MyVHDL.

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. Note: You can compile VHDL Source Code by clicking right mouse button and then choose Compile. Or type *F7* key

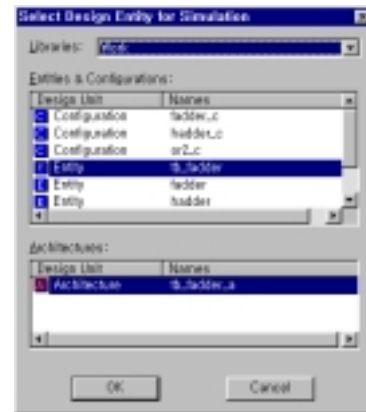
3.5. Prepare Simulation

To prepare simulate VHDL Source Code, just follow from step 1 to step 8.

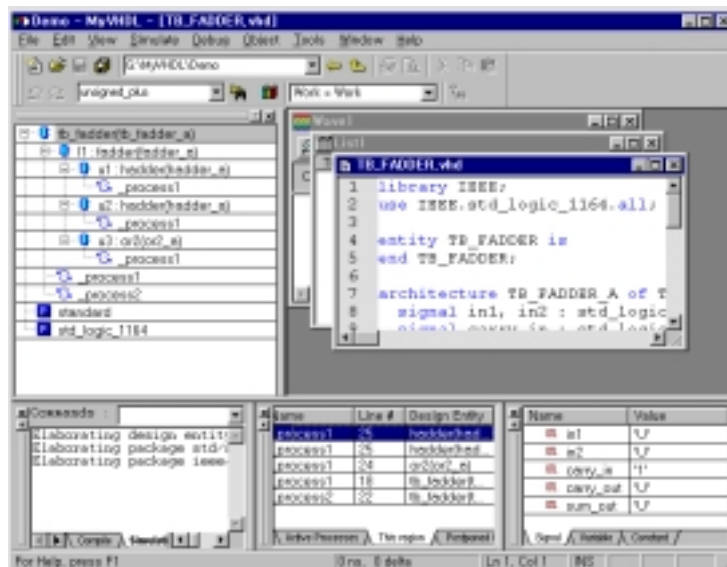
Step 1. Choose *Simulate*→*Simulate(F5)* at pop-up menu of MyVDHL.

Then Select Design Entity for Simulation dialog box will be shown.

Step 2. Select TB_Adder which contains test bench code from Entities & Configurations list box.



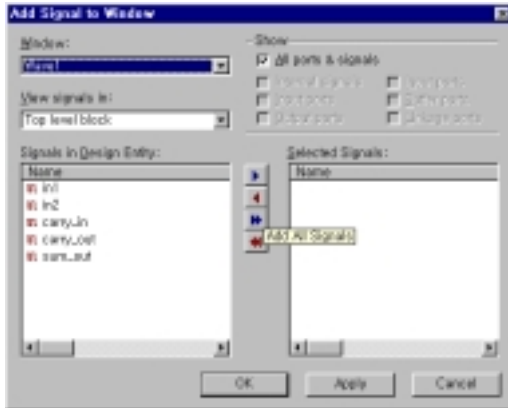
Step 3. MyVHDL GUI is changed to Simulation Mode.




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Step 4. To proceed, you have to *add object*. To *add object*, choose *Object*→*Add Object* to pop-up menu of MyVHDL.



Then, Add Signals to Window will be shown like following. Select signals that you want to see the waveform from Signals in Design Entity list box.

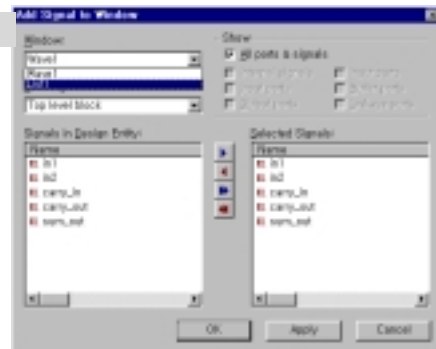


Step 5. Choose Wave at Window input box, and *Top level block* at View Signal in text input box.

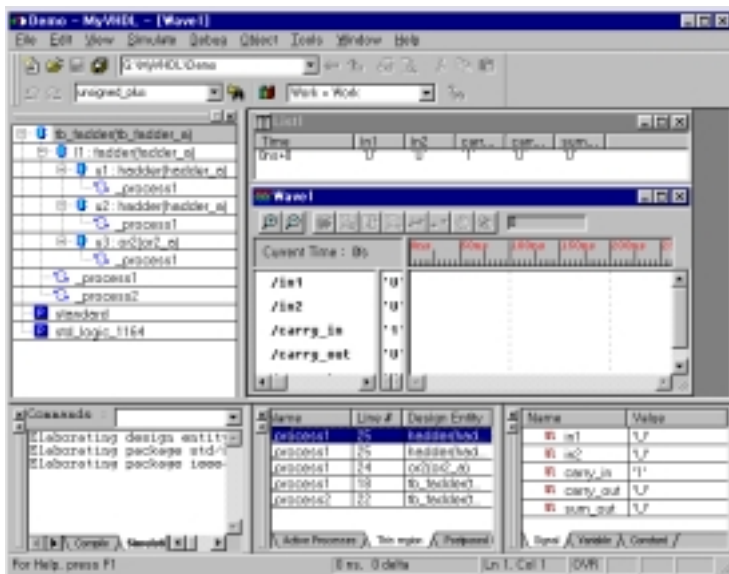
Step 6. To add signal to waveform window, you have to move signals from *Signals in Design Entity* list box to *Selected Signals* list box. To move a signal to *Selected Signs* list box, select the signal, which you want to add from *Signals in Design Entity* list box. And click  .

If you want to remove a signal at *Selected Signals* list box, select it and click .

Step 7. If you want to move all signals to Selected Signals list box, click . If you click , then all signals in *Selected Signals* list box will be removed.



Step 8. To proceed, click *Apply*.



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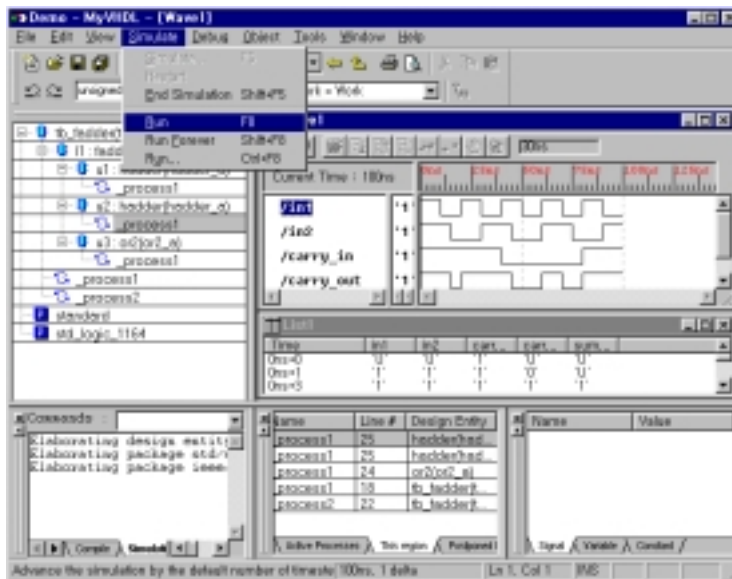
3.6. Run Simulation

MyVHDL can perform either continuous simulation or source code debugging.

To run simulation continuously, choose **Simulation** → **Run** (*Ctrl + F8*) at pop-up menu of MyVHDL. Then, Simulation Time dialog box will be shown.



Type 30 ns to Simulation time text input box.



3.7. Debug

To debug VHDL source code, follow from step 1 to step 5.

MyVHDL Station Tutorial

Step 1. Choose *Debug* → *Break (Break)* at pop-up menu of MyVHDL.

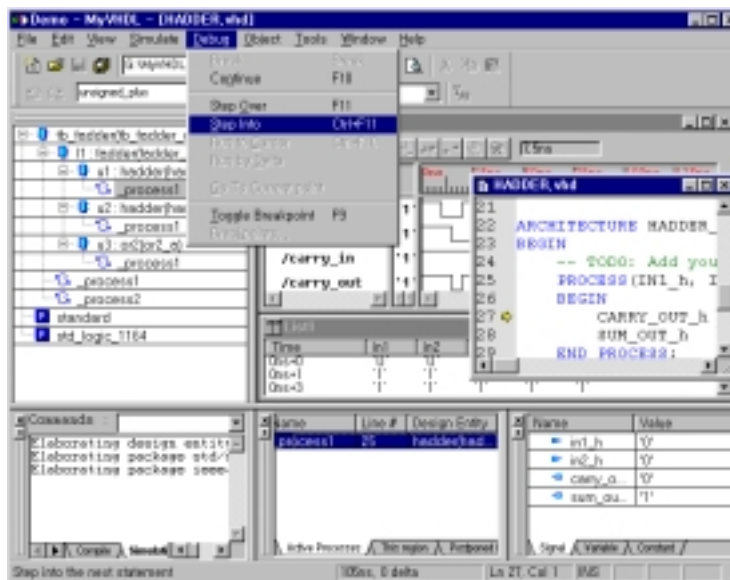
To debug source code, you have to stop simulation

Step 2. You have to set breakpoints for specifying debugging region. To set breakpoints, choose *Debug* → *BreakPoint (F9)* at pop-up menu of MyVHDL. Then ● mark will be added to line number and ◐ mark will be added.

Step 3. To run debugger, choose *Debug* → *Continue (F10)* at pop-up menu of MyVHDL.

Step 4. If you want to debug a present level, choose *Debug* → *Step over (F11)* at pop-up menu of MyVHDL.

Step 5. If you want simultaneous debug from top-level to button-level, choose *Debug* → *Step into (Ctrl+F11)* at pop-up menu of MyVHDL.



4. Close MyVHDL Station

To close MyVHDL Station, choose *File* → *Exit* at the pop-up menu of MyVHDL.
